Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Previously Presented): A signal processing device for processing a received signal to generate a sliced signal, comprising:

an equalizer for generating an equalized signal according to the received signal;

a multilevel quantizer coupled with the equalizer for selectively utilizing a first amount of one or more thresholds or a second amount of one or more thresholds to quantize the equalized signal in order to generate the sliced signal, wherein the first amount is different from the second amount; and

a control logic for controlling the multilevel quantizer to quantize the equalized signal by the first amount of threshold/thresholds or the second amount of threshold/thresholds;

wherein the control logic controls the multilevel quantizer by executing the following steps:

comparing the equalized signal with a predetermined level for a first difference;

comparing the equalized signal with a predetermined constant for a second difference;

controlling the multilevel quantizer to quantize the equalized signal by the first amount of threshold/thresholds for the sliced signal, in the case of the first difference and the second difference having the same sign (positive/negative); and

controlling the multilevel quantizer to quantize the equalized signal by the second amount of threshold/thresholds for the sliced signal, in the case of the first difference and the second difference having different signs (positive/negative).

Claim 2 (Previously Presented): The device of claim 1 wherein the equalizer comprises a feed-forward equalizer (FFE), a feed-back equalizer (FBE), and an adder coupled respectively with the FFE and the FBE for outputting the equalized signal according to signals outputted from the FFE and the FBE.

Claim 3 (Previously Presented): The device of claim 1 further comprising:
a derotator coupled between the equalizer and the multilevel quantizer for derotating the equalized signal and inputting the derotated equalized signal into the multilevel quantizer; and
a rotator coupled between the multilevel quantizer and the equalizer for rotating the sliced signal outputted from the multilevel quantizer and inputting the rotated sliced signal into the equalizer.

Claim 4 (Previously Presented): The device of claim 3 wherein the rotator is coupled with a feed-back equalizer of the equalizer for rotating the sliced signal, and the rotated sliced signal is a passband signal.

Claims 5-7 (Cancelled)

Claim 8 (Previously Presented): The device of claim 1 wherein the predetermined constant is determined by a constant modulus algorithm.

Claim 9 (Previously Presented): The device of claim 1 wherein the control logic controls the multilevel quantizer according to the following steps:
controlling the multilevel quantizer to quantize the equalized signal by the first amount of threshold/thresholds for the sliced signal, in the case of the first difference being less than a predetermined value, and the first difference and the second difference have the same sign (positive/negative); and

controlling the multilevel quantizer to quantize the equalized signal by the second amount of threshold/thresholds for the sliced signal, in the case of the first difference being larger than the predetermined value and the first difference and the second difference have different signs (positive/negative).

Claim 10 (Cancelled)

Claim 11 (Original): The device of claim 1 wherein the sliced signal output by the multilevel quantizer has a plurality of bits.

Claim 12 (Previously Presented): A signal processing device for generating a sliced signal according to a received signal, comprising:

an equalizer for generating an equalized signal according to the received signal;

a quantizer, coupled to the equalizer, for generating the sliced signal according to the equalized signal and a first amount of threshold/thresholds when a first slice mode is applied, and generating the sliced signal according to the equalized signal and a second amount of threshold/thresholds when a second slice mode is applied; and

a control logic, coupled to the quantizer, for controlling the quantizer to apply the first slice mode or the second slice mode through executing the following steps:

subtracting the equalized signal from a predetermined level to obtain a first value;

determining whether the quantizer is in a first status or a second status according to the first value;

if the quantizer is in the first status, controlling the quantizer to apply the first slice mode; and

if the quantizer is in the second status, controlling the quantizer to apply the second slice mode;

wherein the first amount of threshold/thresholds is different from the second amount of threshold/thresholds.

Claim 13 (Previously Presented): The signal processing device of claim 12, wherein the control logic further executes the following step:

determining whether the first value is less than a predetermined value, so as to determine that the quantizer is in the first status or second status.

Claim 14 (Previously Presented): The signal processing device of claim 12, wherein the control logic further executes the following steps:

subtracting the equalized signal from a predetermined constant to obtain a second value; and

comparing the first value with the second value, so as to determine whether the quantizer is in the first status or second status.

Claim 15 (Previously Presented): The signal processing device of claim 14, wherein the control logic compares the first value with the second value, so as to determine whether the first and second values have the same attribute and thereby determine that the quantizer is in the first status or second status.

Claim 16 (Previously Presented): The signal processing device of claim 12, wherein the first status represents that the sliced signal is substantially correct, the second status represents that the sliced signal is substantially incorrect, and the first amount of threshold/thresholds is less than the second amount of threshold/thresholds.

Claim 17 (Previously Presented): A signal processing method for generating a sliced signal according to a received signal, comprising:

generating an equalized signal according to the received signal;

generating the sliced signal according to the equalized signal and a first amount of threshold/thresholds when a first slice mode is applied, and generating the sliced signal according to the equalized signal and a second amount of threshold/thresholds when a second slice mode is applied; and

applying one of the first slice mode and the second slice mode according to the following steps:

subtracting the equalized signal from a predetermined level to obtain a first value;

determining whether the sliced signal is substantially correct or substantially incorrect according to the first value;

if the sliced signal is substantially correct, applying the first slice mode; and

if the sliced signal is substantially incorrect, applying the second slice mode;

wherein the first amount of threshold/thresholds is different from the second amount of threshold/thresholds.

Claim 18 (Previously Presented): The method of claim 17, further comprising the following step:

determining whether the first value is less than a predetermined value, so as to determine that the sliced signal is substantially correct or substantially incorrect.

Claim 19 (Previously Presented): The method of claim 17, further comprising the following steps:

subtracting the equalized signal from a predetermined constant to obtain a second value; and

comparing the first value with the second value, so as to determine that the sliced signal is substantially correct or substantially incorrect.

Claim 20 (Previously Presented): The method of claim 19, further comprising:

comparing the first value with the second value, so as to determine whether the first and second values have the same attribute and thereby determine that the sliced signal is substantially correct or substantially incorrect.

Claim 21 (New): The device of claim 1, wherein the multilevel quantizer utilizes the first amount of the threshold/thresholds to quantize the equalized signal to generate the sliced signal with a first number of bit/bits, and utilizes the second amount of the threshold/thresholds to quantize the equalized signal to generate the sliced signal with a second number of bit/bits which is different from the first number of bit/bits.

Claim 22 (New): The device of claim 1, wherein all of the thresholds for the multilevel quantizer remain the same while the equalized signal varies.

Claim 23 (New): The signal processing device of claim 12, wherein the quantizer generates the sliced signal with a first number of bit/bits when the first slice mode is applied, and generates the sliced signal with a second number of bit/bits which is different from the first number of bit/bits when the second slice mode is applied.

Claim 24 (New): The signal processing device of claim 12, wherein all of the thresholds for the quantizer remain the same while the equalized signal varies.

Claim 25 (New): The method of claim 17, further comprising:

generating the sliced signal with a first number of bit/bits when the first slice mode is applied; and

generating the sliced signal with a second number of bit/bits which is different from the first number of bit/bits when the second slice mode is applied.

Claim 26 (New): The method of claim 17, wherein all of the thresholds for generating the sliced signal remain the same while the equalized signal varies.